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Source: Category:DownloadexFIG. 1 illustrates an example of a conventional DLL. Referring to FIG. 1, a phase-locked loop (PLL) circuit 10 includes a voltage-controlled oscillator (VCO) 12, a phase detector 14, a loop filter 16, and a charge pump circuit 18. The VCO 12 outputs a reference clock CLKX to the phase detector 14 at a frequency fVCOX. The phase detector 14 detects the phase difference between the reference clock CLKX and an output clock CLKD from the VCO 12. Based on the detected phase difference, the phase detector 14 generates a pulse having a width corresponding to the detected phase difference. The pulse from the phase detector 14 is filtered by the loop filter 16. Based on the pulse from the phase detector 14, the charge pump circuit 18 generates a voltage VDIF to control the frequency of the VCO 12. The VCO 12 outputs the output clock CLKD in response to the voltage VDIF from the charge pump circuit 18. The PLL circuit 10 generates the output clock CLKD in response to the reference clock CLKX and is therefore advantageous in that the output clock CLKD is synchronized with the reference clock CLKX. FIG. 2 is a timing diagram illustrating a conventional operation of the PLL circuit 10. Referring to FIG. 2, when the reference clock CLKX transitions to the high level from the low level, the VCO 12 initially outputs the reference clock CLKX at a constant frequency. Subsequently, when the reference clock CLKX transitions to the low level, the phase detector 14 detects a phase difference corresponding to the output clock CLKD. Then, when the phase detector 14 detects the phase difference corresponding to the output clock CLKD, the phase detector 14 generates a pulse having a width corresponding to the detected phase difference. The pulse generated by the phase detector 14 is input to the loop filter 16, and is smoothed by the loop filter 16. Based on the smoothed pulse, the charge pump circuit 18 outputs the voltage VDIF to control the frequency of the VCO 12, so that the VCO 12 outputs the output clock CLKD. FIG. 3 is a block diagram of a conventional external circuit, such as a memory controller, to which the PLL circuit 10 is coupled. Referring to FIG. 3, the PLL circuit 10 includes an input buffer 11, 2d92ce491b